

CLAIMS:

1. A microelectronic device fabricating method comprising:
providing a substrate having a mean global outer surface extending
along a plane;

forming a first portion over the substrate comprising a substantially straight linear segment which is angled from the plane and forming a second portion over the substrate comprising a substantially straight linear segment which is angled from the plane at a different angle than the first portion;

forming a layer of structural material over the first and second portions; and

anisotropically etching the structural material layer and leaving a first device feature over the first portion having a first base width and leaving a second device feature over the second portion having a second base width which is different from the first base width.

2. The method of claim 1 comprising forming the layer of structural material to be electrically conductive.

3. The method of claim 1 comprising forming the layer of structural material to be electrically insulative.

1 4. The method of claim 1 comprising forming the layer of
2 structural material to be semiconductive.

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4 5. The method of claim 1 comprising forming the first portion
5 to comprise elongation in a direction generally parallel with the plane,
6 forming the layer of structural material to be electrically conductive, and
7 anisotropically etching the electrically conductive structural material to
8 form a pair of elongated conductive interconnect lines having different
9 base widths.

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11 6. The method of claim 1 wherein the layer comprises multiple
12 discrete layers.

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14 7. The method of claim 1 wherein the first portion straight
15 linear segment extends to an outermost surface portion which is planar
16 and parallel with the plane.

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18 8. The method of claim 1 wherein the first portion straight
19 linear segment is not perpendicular with the plane, and extends to an
20 outermost surface portion which is planar and parallel with the plane.

1 9. The method of claim 1 wherein the first portion straight
2 linear segment extends to an outermost surface portion which is planar
3 and parallel with the plane, and wherein the second portion straight
4 linear segment extends to an outermost surface portion which is planar
5 and parallel with the plane.

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7 10. The method of claim 1 wherein the first portion straight
8 linear segment extends to an innermost surface portion which is planar
9 and parallel with the plane, and wherein the second portion straight
10 linear segment extends to an innermost surface portion which is planar
11 and parallel with the plane.

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13 11. The method of claim 1 wherein both the first and second
14 linear segments are beveled relative to the plane.

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16 12. The method of claim 1 wherein only one of the first and
17 second linear segments is beveled relative to the plane.

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19 13. The method of claim 1 wherein the forming of at least one
20 of the first portion and the second portion comprises forming a mask
21 having a sloped resist sidewall over material from which the one is
22 formed, and etching the resist and said material.

1 14. A microelectronic device fabricating method comprising:
2 providing a substrate having a mean global outer surface extending
3 along a plane;
4 forming a first portion over the substrate comprising a
5 substantially straight linear segment which is angled from the plane and
6 forming a second portion over the substrate comprising a substantially
7 straight linear segment which is angled from the plane at a different
8 angle than the first portion, the first portion straight linear segment
9 extending to an outermost surface portion which is planar and parallel
10 with the plane, the second portion straight linear segment extending to
11 an outermost surface portion which is planar and parallel with the
12 plane, the first portion straight linear segment extending to an innermost
13 surface portion which is planar and parallel with the plane, the second
14 portion straight linear segment extending to an innermost surface portion
15 which is planar and parallel with the plane;
16 forming a layer of structural material over the first and second
17 portions; and
18 anisotropically etching the structural material layer and leaving a
19 first device feature over the first portion having a first base width and
20 leaving a second device feature over the second portion having a second
21 base width which is different from the first base width.
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1 15. The method of claim 14 comprising forming the layer of
2 structural material to be electrically conductive.

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4 16. The method of claim 14 comprising forming the first portion
5 to comprise elongation in a direction generally parallel with the plane,
6 forming the layer of structural material to be electrically conductive, and
7 anisotropically etching the electrically conductive structural material to
8 form a pair of elongated conductive interconnect lines having different
9 base widths.

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11 17. The method of claim 14 wherein both the first and second
12 linear segments are beveled relative to the plane.

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14 18. The method of claim 14 wherein only one of the first and
15 second linear segments is beveled relative to the plane.

1 19. A method of forming a pair of field effect transistor gate
2 lines of different base widths from a common deposited conductive
3 layer, comprising:

4 providing a substrate having a mean global outer surface extending
5 along a plane;

6 forming a first mandril over the substrate having a first portion
7 comprising a substantially straight linear segment which is angled from
8 the plane and forming a second mandril over the substrate comprising
9 a substantially straight linear segment which is angled from the plane
10 at a different angle than the first portion;

11 forming a gate dielectric layer over the substrate;

12 depositing a conductive gate layer over the first and second
13 portions of the first and second mandrils and over the gate dielectric
14 layer; and

15 anisotropically etching the conductive gate layer and forming a
16 first gate line over the first portion having a first base gate width and
17 forming a second gate line over the second portion having a second
18 base gate width which is different from the first base width.

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20 20. The method of claim 19 wherein the gate dielectric layer
21 is formed prior to forming the first and second mandrils, and the first
22 and second mandrils are formed over the gate dielectric layer.

1 21. The method of claim 19 wherein the gate dielectric layer
2 is formed after forming the first and second mandrels.

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4 22. The method of claim 19 wherein the conductive gate layer
5 comprises multiple discrete layers.

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7 23. The method of claim 19 wherein the first portion straight
8 linear segment extends to an outermost surface portion which is planar
9 and parallel with the plane.

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11 24. The method of claim 19 wherein the first portion straight
12 linear segment is not perpendicular with the plane, and extends to an
13 outermost surface portion which is planar and parallel with the plane.

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15 25. The method of claim 19 wherein the first portion straight
16 linear segment extends to an outermost surface portion which is planar
17 and parallel with the plane, and wherein the second portion straight
18 linear segment extends to an outermost surface portion which is planar
19 and parallel with the plane.

1 26. The method of claim 19 wherein the first portion straight
2 linear segment extends to an innermost surface portion which is planar
3 and parallel with the plane, and wherein the second portion straight
4 linear segment extends to an innermost surface portion which is planar
5 and parallel with the plane.

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7 27. The method of claim 19 wherein both the first and second
8 linear segments are beveled relative to the plane.

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10 28. The method of claim 19 wherein only one of the first and
11 second linear segments is beveled relative to the plane.

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13 29. The method of claim 19 comprising forming the first and
14 second mandrels to be electrically insulative.

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16 30. The method of claim 19 comprising after the anisotropic
17 etching, etching at least portions of the first and second mandrels from
18 the substrate.

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20 31. The method of claim 19 comprising after the anisotropic
21 etching, etching all of the first and second mandrels from the substrate.

1 32. The method of claim 19 comprising after the anisotropic
2 etching, etching only portions of the first and second mandrels from the
3 substrate and leaving portions of the first and second mandrels as part
4 of the finished circuitry.

5
6 33. A method of forming a pair of conductive device
7 components of different base widths from a common deposited
8 conductive layer, comprising:

9 providing a substrate having a mean global outer surface extending
10 along a plane;

11 forming a first mandrel over the substrate having a first portion
12 comprising a substantially straight linear segment which is angled from
13 the plane and forming a second portion over the gate dielectric layer
14 comprising a substantially straight linear segment which is angled from
15 the plane at a different angle than the first portion;

16 depositing a conductive layer over the first and second portions
17 of the first and second mandrels;

18 anisotropically etching the conductive layer and forming a first
19 conductive device component over the first portion having a first base
20 width and forming a second device component having a second base
21 width which is different from the first base width; and

22 after the anisotropic etching, etching at least portions of the first
23 and second mandrels from the substrate.

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1 34. The method of claim 33 comprising forming the first and
2 second mandrels to be electrically insulative.

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4 35. The method of claim 33 comprising after the anisotropic
5 etching, etching all of the first and second mandrels from the substrate.

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7 36. The method of claim 33 comprising after the anisotropic
8 etching, etching only portions of the first and second mandrels from the
9 substrate and leaving portions of the first and second mandrels as part
10 of the finished circuitry.

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12 37. The method of claim 33 comprising forming the first and
13 second conductive device components to be electrically conductive lines.

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15 38. The method of claim 33 comprising forming the first and
16 second conductive device components to be field effect transistor gates.

1 39. Integrated circuitry comprising:

2 a substrate having a mean global outer surface extending along
3 a plane;

4 the substrate comprising a first conductive device component of
5 a first type and being elongated in a first direction generally parallel
6 with the plane;

7 a second conductive device component of the first type and being
8 elongated in a second direction generally parallel with the plane, the
9 first and second conductive device components at least predominately
10 comprising common conductive material; and

11 the first and second conductive device components having different
12 base widths, at least one of the first and second conductive device
13 components having a mean elevational axis which is angled from
14 perpendicular to the plane along at least a majority of its elongated
15 length in its respective first or second direction.

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17 40. The integrated circuitry of claim 39 wherein the first and
18 second directions are parallel with one another.

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20 41. The integrated circuitry of claim 39 wherein the first and
21 second directions are not parallel with one another.

1 42. The integrated circuitry of claim 39 wherein the first and
2 second conductive device components entirely comprise common
3 conductive material in at least one cross section.

4 43. The integrated circuitry of claim 39 wherein both the first
5 and the second conductive device components have a respective mean
6 elevational axis which is elevationally angled from perpendicular to the
7 plane along at least a majority of its elongated length in its respective
8 first or second direction.

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11 44. The integrated circuitry of claim 39 wherein both the first
12 and second conductive device components have mean elevational axes
13 which are differently elevationally angled from the plane, the first or
14 second conductive device component having the lesser angle from the
15 plane having a shorter base width than the first or second conductive
16 device component having the greater angle from the plane.

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18 45. The integrated circuitry of claim 39 wherein only one of the
19 first and the second conductive device components has a mean
20 elevational axis which is angled from perpendicular to the plane.

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